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| 10/004,197 | 11/14/2001 | Craig Nemecek | CYPR-CD01220M | 1794 |

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| EXAMINER | |
|---|---|
| PROCTOR, JASON SCOTT | |
| **ART UNIT** | **PAPER NUMBER** |
| 2123 | |

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/004,197 | NEMECEK ET AL. | |
| | Examiner | Art Unit | |
| | Jason Proctor | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-21* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-21 were rejected in Office Action of 23 November 2005.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9 January 2006 has been entered.

Claims 1, 7, 13, 17, 19, and 21 have been amended. Claims 1-21 remain pending in this application.

Claims 1 and 3-21 have been rejected. Claim 2 has been objected to.

### *Claim Objections*

1. Claim 13 is objected to because of the following informalities: The limitation "upon execution of the break command permitting the host computer to have access to registers and memory locations in the virtual microcontroller" lacks clarity by omitting a comma between "command" and "permitting." Compare to claim 21. Appropriate correction is required.

2. Claim 13 is objected to because of the following informalities: The format of claim 13 renders it unclear what the object of the method is. For example, the step "receiving a halt command" implies that something is receiving the halt command, but it is unclear what that object is. Does the gatekeeper receive a halt command? The host computer? Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 3-21 are rejected under 35 U.S.C. § 102(e) as being anticipated by US Patent No. 6,366,878 to Grunert.

Regarding claim 1, Grunert discloses:

An In-Circuit Emulation system [*"a circuit arrangement for in-circuit emulation"* (column 1, lines 66-67)], comprising:

A microcontroller [*"comprising a first ... microcontroller"* (column 1, line 66 – column 2, line 1)] having a microcontroller clock [*"a clock synchronizes the two microcontrollers (2, 3)"* (column 2, lines 58-59)];

A virtual microcontroller [*"comprising ... a second microcontroller"* (column 1, line 66 – column 2, line 1)] running in lock-step synchronization with the microcontroller [*"a clock synchronizes the two microcontrollers (2, 3)"* (column 2, lines 58-59)] by executing the same instructions [*"The microcontrollers have an ROM memory 8, 8' in which the operating program is otherwise stored in normal operation. During in-circuit emulation, the memory 8, 8' is switch off... The master 2 is connected to the external memory 4 by means of its ports P0, P2... The data D read out from the memory 4 are also fed to the slave 3."* (column 4, lines 29-53); That is, during in-circuit emulation, both microcontrollers (2, 3) receive the same operating program from external memory 4, thus execute the same instructions.] using the same clocking signals between said microcontroller and said virtual microcontroller [*"A clock system 5 ensures good synchronization between master 2 and slave 3."* (column 5, lines 8-9); *"a clock synchronizes the two microcontrollers (2, 3)."* (column 2, lines 58-59)];

A gatekeeper circuit coupled to the virtual microcontroller and the microcontroller [*"The microcontroller 2 is operated as master, the microcontroller 3 as slave."* (column 4, lines 37-39); *"The corresponding ports P5', P6', are therefore free in the slave 3, with the result that they can be used for inputting and outputting further internal signals and states, for example internal buses, control signals, register contents, etc. or for controlling the program execution. Internal states of the master 2 are transmitted to the slave 3 via the ports P3, P4', and then to the service computer via the ports P5', P6', ...* [sic] *The contents of the memory 4 can be changed by the service computer, in order to optimize the microcontroller in the application system during the development phase."*

(column 5, lines 13-23); The ports P5', P6', are functionally equivalent to the claimed gatekeeper circuit as described above and elsewhere by Grunert.];

A host computer running In-Circuit Emulation debug software [*"The emulation operation is controlled by means of a service computer connected to the circuit arrangement 1."* (column 5, lines 9-10)], the host computer being in communication with the gatekeeper circuit (column 5, lines 13-23) so that halt commands and requests for data from the virtual microcontroller are passed through and regulated by the gatekeeper circuit to assure that emulator operations are not disturbed [Grunert contains no explicit disclosure that halt commands and requests for data "disturb emulator operations."]

Regarding claims 3 and 6, Grunert discloses that the gatekeeper circuit comprises means for determining that the microcontroller is in a sleep state [*"The corresponding ports P5', P6' ... can be used for inputting and outputting further internal signals and states, for example ... control signals, register contents, etc. or for controlling the program execution. Internal states of the master 2 are transmitted to the slave 3 via the ports P3, P4', and then to the service computer via the ports P5', P6'"* (column 5, lines 12-19) A "sleep state" is clearly an "internal state" of the master 2 (microcontroller), which states are transmitted via the functional equivalent of the gatekeeper circuit.]

Grunert discloses that the gatekeeper circuit further comprises means for notifying the host computer of the microcontroller's state in the event the microcontroller is in a sleep state (column 5, lines 12-19).

Regarding claim 4, Grunert discloses that the gatekeeper circuit determines that the microcontroller is in the sleep state by determining if the microcontroller clock is operating [*"a clock synchronizes the two microcontrollers (2, 3)"* (column 2, lines 58-59); The gatekeeper circuit inherently "determines if the microcontroller clock is operating" because if that clock is not operating, the gatekeeper circuit is not operating.]

Regarding claim 5, Grunert discloses that the gatekeeper circuit determines that the microcontroller is in the sleep state by determining if the microcontroller clock is operating and a data line from the microcontroller is in a prescribed logic state [*"a clock synchronizes the two microcontrollers (2, 3)"* (column 2, lines 58-59); The gatekeeper circuit inherently "determines if the microcontroller clock is operating" because if that clock is not operating, the gatekeeper circuit is not operating. *"microcontrollers (2, 3) in each case have circuit means which can be used to interrogate the signal level present during a reset operation, and wherein the signal levels at the first and second microcontrollers (2, 3) are different"* (column 3, lines 5-13); Clearly Grunert discloses detecting logic states on data lines. Further, the limitation "a data line from the microcontroller is in a prescribed state" merely recites what is necessary to interface with the microcontroller. In contrast, if Grunert's microntrollers signal that they are in a halt or sleep state with a "random logic state," it would be impossible to detect anything about them and the system would be inoperable.]

Regarding claims 7 and 8, Grunert discloses that the gatekeeper circuit comprises means for determining for receiving a halt command from the host computer and for queuing a break to

the microcontroller and the virtual microcontroller in response thereto [*"The corresponding ports P5', P6' ... can be used for inputting and outputting further internal signals and states, for example, internal buses, control signals, register contents, etc. or for controlling the program execution. Internal states of the master 2 are transmitted to the slave 3 via the ports P3, P4', and then to the service computer via the ports P5', P6', ...* [sic] *The contents of the memory 4 can be changed by the service computer, in order to optimize the microcontroller in the application system during the development phase. The internal state of the master 2 can be traced by setting breakpoints. The service computer executes the application program in this case in parallel with the execution in the master 2."* (column 5, lines 13-25); Applicants' arguments regarding the claim language "queuing" seem to imply that executing a single halt or breakpoint instruction does not constitute a "queue." The Examiner finds this argument unpersuasive and finds no implicit limitation in the term "queuing" that requires a plurality of halt or breakpoint instructions waiting for execution.].

Grunert discloses that the gatekeeper circuit further comprises means for detecting that a break has occurred in the microcontroller and the virtual microcontroller and for notifying the host computer that the break has occurred (column 5, lines 12-25).

Regarding claims 9, 10, and 12, Grunert discloses that the halt command comprises one of a programmed breakpoint and a user initiated manual halt command (column 5, lines 12-25) and wherein the halt command is issued by a breakpoint controller in response to detection of a programmed breakpoint [(column 5, lines 12-25); This claim recites the inherent function implemented to create a "programmed breakpoint." Whatever mechanism implements such a

"programmed breakpoint" becomes a "breakpoint controller," and as disclosed by Grunert, interacts with the microcontrollers (2, 3) to halt either or both microcontroller.]

Regarding claim 11, Grunert discloses that the gatekeeper further comprises means for permitting access to registers and memory locations in the virtual microcontroller when the microcontroller and the virtual microcontroller are in a halted state ["[P5', P6'] *can be used for inputting and outputting further internal signals and states, for example internal buses, control signals, register contents, etc. or for controlling the program execution. Internal states of the master 2 are transmitted to the slave 3 via the ports P3, P4', and then to the service computer via the ports P5', P6"* (column 5, lines 12-19)].

Regarding claim 13, the citations and rationale given above regarding claim 1 are incorporated, and additionally Grunert discloses:

Receiving a halt command and queuing a break command to the microcontroller and the virtual microcontroller in response to the halt command, and upon execution of the break command, permitting the host computer to have access to registers and memory locations in the virtual microcontroller [*"The corresponding ports P5', P6' ... can be used for inputting and outputting further internal signals and states, for example, internal buses, control signals, register contents, etc. or for controlling the program execution. Internal states of the master 2 are transmitted to the slave 3 via the ports P3, P4', and then to the service computer via the ports P5', P6', ...* [sic] *The contents of the memory 4 can be changed by the service computer, in order to optimize the microcontroller in the application system during the development phase.*

*The internal state of the master 2 can be traced by setting breakpoints. The service computer executes the application program in this case in parallel with the execution in the master 2."* (column 5, lines 13-25); Applicants' arguments regarding the claim language "queuing" seem to imply that executing a single halt or breakpoint instruction does not constitute a "queue." The Examiner finds this argument unpersuasive and finds no implicit limitation in the term "queuing" that requires a plurality of halt or breakpoint instructions waiting for execution.]

Applicants' arguments state that "Independent claim 13 is similar in scope to that of independent claim 1," and therefore further specific treatment of claim 13 is considered unnecessary.

Regarding claims 14 and 15, the recited limitations are equivalent to a break in claim 9 and a breakpoint or breakpoint instruction in claim 10. Applicants have not seasonably traversed this interpretation, first put forth in the previous Office Action.

Regarding claim 16, the recited step is inconsequential. There is no positively recited limitation aside from "determining," which is defined generically, and the claim provides for no action to be taken based upon that determination. Therefore claim 16 appears to be equivalent to claim 13, from which it depends, and is rejected for rationale similar to that given above for claim 13.

Regarding claims 17 and 18, the recited limitations are equivalent to those recited in claims 4 and 5. Claims 17 and 18 are therefore rejected for rationale similar to that given above for claims 4 and 5.

Regarding claim 19, the recited limitations are equivalent to those recited in claim 6. Claim 19 is therefore rejected for rationale similar to that given above for claim 6.

Regarding claim 20, the recited limitations are equivalent to those recited in claim 8. Claim 20 is therefore rejected for rationale similar to that given above for claim 8.

Regarding claim 21, this claim recites a combination of limitations found in claims 1, 5-6, and 8-11, which have been rejected above. Further, Applicants' arguments state that "Claim 21 recites the method employed by a system combining the limitations of Claims 5-6 and 8-11 as discussed above." Therefore claim 21 is rejected for similar rationale to that given for claims 1, 5-6, and 8-11 above, and further specific treatment of claim 21 is considered unnecessary.

***Response to Arguments***

Applicants' arguments have been fully considered, but in light of the new grounds of rejection above they are moot.

### *Allowable Subject Matter*

4. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The limitations of claim 2 that "a gatekeeper clock running independent of the microcontroller clock" is not disclosed in the closest prior art. The limitation is supported by the disclosure and exemplified in FIG. 8, reference 610. Although a separate and independent gatekeeper clock may be known in the prior art, such a modification would destroy the Grunert reference because the "gatekeeper circuit" is a component function of microcontroller 3, which is naturally driven by the microcontroller clock 5 (see column 2, lines 58-59; column 5, lines 8-9).

### *Conclusion*

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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Paul L. Rodriguez 3/29/06
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